Optimum Performance of Carbon Nanotube Field Effect Transistor

Soheli Farhana, AHM Zahirul Alam, and Sheroz Khan

***Abstract*—Phenomenological predictions have been elucidated in this paper. The predictions are elaborated for the field effect transistor using carbon nanotube (CNT) technology. CNTs have small band gap compare to other traditional semiconductor technologies. The modeling of a single wall nanotube with optimum bandgap for the designing of the carbon nanotube (CNTFET) is the aim of this work. Analysis of I-V characteristics of CNTFET with the drain current-voltage analytical relation enables the lower energy consumption from the proposed design. In this research, the optimum carbon nanotube (CNTs) is analyzed where the bandgap is 0.45eV as well as the diameter is 1.95nm. Modeling of CNTFET will be useful for semiconductor industries in order to manufacture the nano scale device.**

***Index Terms*—Transistor, I-V, semiconductor, carbon nanotube.**

I. Introduction

DESPITE of the materials are used in processing for electronic device, CNTFET act as a potential component in the nano device production at present as well as in future. Recent rapid progress of carbon nanotube are moving faster to produce CNTFET based integrated circuits. The scaling of the technology cannot be going beyond 22nm, therefore the scaling become very complicated to fabricate nano dimension device [1]. In facts, CNTFET is the substitute of silicon MOS where it shows the very small dimensions and better performances [2,3]. In 1998, researchers have started modeling of CNTFET after discovering the CNTs [4,5]. CNT arrays are used to construct conventional CNTFET [6] with higher "on" currents where the device physics has involved [7,8]. For simulating of million atom nanostructure semiconductor devices, a new empirical pseudo potential calculation approach was proposed [9]. This model solves the transport problem based on an open boundary condition which reduces the computational costs compare to other traditional methods such as TB and NEGF approaches. However, this model fails to show the optimum result rather than to use the other method. Furthermore, an optimum model is required to design CNTFET.

A semi empirical model was developed using quantum mechanics to pass up the route to self-consistency [10]. The semi empirical model of CNTFET is constructed to enable the easy application in the simulator. No validation was shown in this development. But another model is trying to validate using their numerical experimental data [11]. In this paper, a lower bandgap of CNT based FET compact model is proposed and verified, in terms of saturation and leakage current variations with Transconductance.

Manuscript received April 30, 2014; revised May 20, 2014. This work was supported by the Ministry of Higher Education (MOHE) Malaysia through FRGS grant.

Soheli Farhana is with the Electrical and Computer Engineering Department, International Islamic University Malaysia, 53100 Kuala Lumpur, Malaysia (Phone: +60361963384; e-mail: soheli.farhana@live.iium.edu.my, farhana.engineer@ieee.org).

AHM Zahirul Alam is with the Electrical and Computer Engineering Department, International Islamic University Malaysia, 53100 Kuala Lumpur, Malaysia (e-mail: zahirulalam@iium.edu.my).

Sheroz Khan is with the Electrical and Computer Engineering Department, International Islamic University Malaysia, 53100 Kuala Lumpur, Malaysia (e-mail: sheroz@iium.edu.my).

II. Proposed Model

A. Band Structure

The structure of single walled CNTFET is constructed by rolling a graphene. In this proposed model, first the electronic properties are characterized with density of states (DOS). The tight binding model gives the E−k value [12]-[19] to get the energy band-gap,

$$E(k_1, k_2) = V_{pp}\pi \times \sqrt{1 + 2\cos(2\pi k_1) + 2\cos(2\pi k_2) + 2\cos\left(2\pi(k_1 - k_2)\right)} \quad (1)$$

where n and m parameters control k_1 and k_2,

$$k_1 = \frac{q}{N}\left(\frac{2n+m}{d_R}\right), \quad k_2 = \frac{q}{N}\left(\frac{2m+n}{d_R}\right)$$

Hence, the values of $E(k_1, k_2)$ are successively calculated using equation (1). Thus the band gap is,

$$E_G = \frac{2a_{cc}|t|}{d} \approx \frac{0.8eV}{d} \quad (2)$$

Based on the above mentioned two expressions, they are the functions of carbon nanotube.

Generally DOS explains each level energies number of states. When there is specific level of energy DOS at high level a, it means that there are many states which are available for occupation. If a DOS has a value of zero means that no states can be occupied at that certain level of energy. In conclusion, it is the derivative of the number of states with respect to energy. DOS can be represented as follows:

$$D(E) = D_0 \frac{|E|}{\sqrt{E^2 - (E_G/2)^2}} \Theta\left(|E| - \frac{E_G}{2}\right) \quad (3)$$

where

ISBN: 978-988-19252-0-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

$$D_0 = \frac{8}{3\pi a_{cc}|t|}$$

B. CNTFET Modeling

Figure 1 shows a CNTFET model which consists of an optimum CNT. Three capacitors are attached as terminals. A charge is placed at the top of the barrier, as shown in Fig.

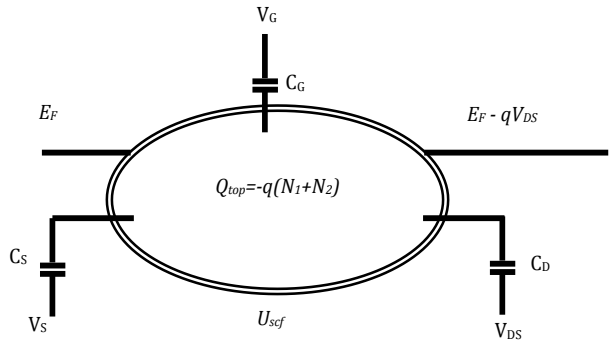

Fig. 1. CNTFET model with three terminals connected by capacitors.

1,. The top of the barrier's local density of states (LDOS) indicates the charge by the self-consistent potential.

The top barrier's equilibrium electron density is N_0 at terminal biases are zero, is,

$$N_O = \int_{-\infty}^{\infty} D(E) f(E - E_f) dE \quad (4)$$

The local density of states is denoted by $D(E)$ and equilibrium Fermi function is denoted by $f(E - E_f)$. Two scenarios may be observed once a bias is supplied to the terminal of gate and drain:

i) two different Fermi levels are realized in the top of the barrier.

ii) The top of the barrier's self-consistent potential is U_{scf}.

$$I_R \text{ or } N_1 = \int_{-\infty}^{\infty} eD(E)V(E)f(E - E_f^L)dE = \int_{-\infty}^{\infty} D(E - U_{scf})f(E - E_f^L)dE \quad (5)$$

$$I_L \text{ or } N_2 = -\int_{-\infty}^{\infty} eD(E)V(E)f(E - E_f^R)dE = -\int_{-\infty}^{\infty} D(E - U_{scf})f(E - E_f^R)dE \quad (6)$$

In equations (2) and (3), $E_f^L = E_f$ and $E_f^R = E_f - qV_{DS}$. These equations can be expressed in a way with the changed variable as follows:

$$N_1 = -\int_{-\infty}^{\infty} D(E) f_R(E) dE \quad (7)$$

$$N_2 = \int_{-\infty}^{\infty} eD(E) f_L(E) dE \quad (8)$$

Where, $f_R(E) = f(E + U_{scf} - E_f^R)$ and, $f_L(E) = f(E + U_{scf} - E_f^L)$.

With the known potential, the top barrier electron density can be calculated as $N=N_1+N_2$. The bias induced charge $\Delta N=(N_1+N_2)-N_0$ at their terminal in Fig. 1. Laplace potential can be calculated for terminal biases by,

$$U_L=-q(\alpha_G V_G+ \alpha_D V_D+ \alpha_S V_S) \quad (9)$$

α_G, α_D and α_S refer the control of Laplace solution from the gate, drain and source. It can be expressed by,

$$\alpha_G = \frac{C_G}{C_\Sigma}, \quad \alpha_D = \frac{C_D}{C_\Sigma}, \quad \alpha_S = \frac{C_S}{C_\Sigma}$$

Short the three terminals to the ground is the solution of second part. Then calculate the top barrier potential of charge by,

$$U_P = \frac{q^2}{C_\Sigma}\Delta N \quad (10)$$

Here U_L is expressed as the top barrier potential and U_P is expressed as the top barrier charge. Now the final solution can be achieved by U_{scf},

$$U_{scf} = U_L + U_P = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C \Delta N \quad (11)$$

In equation (8) the charging energy is denoted by U_c, $U_C = \frac{q^2}{C_\Sigma}$.

The top barrier self consistent potential and electron carrier density can be found using the solution of the above equations. The total left and right currents calculate the conductor current as follows:

$$I = I_R + I_L = \int_{-\infty}^{\infty} eD(E)v(E)\left[f(E - E_F^L) - f(E - E_F^R)\right]dE \quad (12)$$

$$D(E) = \frac{1}{\pi}\left|\frac{d\varepsilon}{dk}\right|^{-1} \quad (13)$$

Velocity becomes,

$$V(E) = \frac{1}{h}\frac{d\varepsilon}{dk} \quad (14)$$

Equation (12) becomes,

$$I = \frac{2e}{h}\int_{-\infty}^{\infty}\left[f(E - E_F^L) - f(E - E_F^R)\right]dE \quad (15)$$

$eV = E_F^L - E_F^R$ it reduces for small biases,

$$I = \left[\frac{2e^2}{h}\int_{-\infty}^{\infty}\left(-\frac{dF}{dE}\right)dE\right]v \quad (16)$$

$G = \frac{1}{v}$ can be expressed as small biases, thus the equation (16) becomes,

$$I = \frac{2e^2}{h}\int_{-\infty}^{\infty}\left(-\frac{dF}{dE}\right)dE \quad (17)$$

Quantum conductance can be acquired at 0^0C,

$$G_0 = \frac{2e^2}{h} \quad (18)$$

Real system transport elaboration consists of two simplifications from above derivations.

Each mode from several modes that donate one quantum to the current.

The other simplification is the unity gain becomes greater than electron transmission possibility due to conductor scattering process. Finally, the equivalent current becomes,

$$I = \frac{2e}{h}\sum_m \int_{-\infty}^{\infty} T_m(E)\left[f(E - E_F^L) - f(E - E_F^R)\right]dE \quad (19)$$

ISBN: 978-988-19252-0-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

Following equation (20) provides the equivalent conductance,

$$G = \frac{2e^2}{h}\sum_m \int_{-\infty}^{\infty} T_m(E)\left(-\frac{\delta F}{\delta E}\right) dE \quad (20)$$

The linear response conductance computing can be done for the sake of two sub-bands for semi-conducting CNTs at the Fermi energy,

$$G = \frac{2e^2}{h} \times 2 = \frac{4e^2}{h} = \frac{1}{6.5\,k\Omega}$$

At last the calculation of the current becomes,

$$I = \frac{4e^2}{h}\int_{-\infty}^{\infty}\left[f\left(E - E_F^L\right) - f\left(E - E_F^R\right)\right]dE \quad (21)$$

$$I_{ds} = \frac{8ekT}{h}\int_{-\infty}^{\infty}\left[\exp\left(\frac{E - E_F^L}{kT}\right) - \exp\left(\frac{E - E_F^R}{kT}\right)\right] \quad (22)$$

C. Optimization of CNTFET I-V Characteristics

Analysis of drain current is the key factor for the optimization, thus the theory and process of calculating it is as follows:

1) Let V_S is grounded for facilitating the analysis of V_G, V_S, V_D and E_F.

2) Laplace potential is calculated using $U_L = -q(\propto_G V_G + \propto_D V_D + \propto_S V_S)$ where $\propto_G = \frac{C_G}{C_\Sigma}, \propto_D = \frac{C_D}{C_\Sigma}, \propto_S = \frac{C_S}{C_\Sigma}$. The term refers to the control parameter of a terminal and C_Σ refers to the total capacitance of the gate, drain and source.

3) The charges are from the positive state filled by the source NS and that of negative velocity states filled by the drain ND,

$$U_P = \frac{q^2}{C_\Sigma}(N_S + N_D) - N_0 \quad (23)$$

where q represents the electronic charge. Therefore, the equilibrium electron density is

$$N_0 = \int_{-\infty}^{\infty} D(E) f(E - E_F) dE \quad (24)$$

where $D(E)$ represents the density of states and $f(E)$ represents the probability that a states with energy level E will occupy.

4) The summation of U_P and U_L equates to U_{scf} which refers to the self-consistent potential for a given charge density.

$$U_{scf} = U_L + U_P$$
$$= -q(\propto_G V_G + \propto_D V_D + \propto_S V_S) + \frac{q^2}{C_\Sigma}(N_S + N_D) - N_0$$

5) Finally, the drain current is computed based on the self-consistent potential profile.

$$I_D = \frac{4qK_BT}{h}\left[In\left(1 + \exp\left(E_F - U_{scf}\right)\right) - In\left(1 + \exp\left(E_F - U_{scf}\right)\right)\right] \quad (25)$$

Where kB is the Boltzman constant, T is the operating temperature, and h is the Planck constant. EF is the Fermi energy, Uscf is also known as the channel surface potential and q shows the charge of electric field.

D. CNTFET Threshold Voltage

Threshold voltage is known as the voltage required to switch on a transistor. Therefore, the threshold voltage is given by,

$$V_{TH} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \quad (26)$$

Where the carbon to carbon atom distance, a = 2.49 Å, the carbon π-π bond energy in the tight bonding model Vπ =3.033 eV, the unit electron charge is e. The CNT diameter is denoted by DCNT. This model shows the diameter of (25, 0) CNT is 1.95 nm, energy gap (Eg) is 0.44eV, the threshold voltage of a CNTFET using (25,0) CNTs as channels is 0.2V from Equation (26).

III. Result and Discussion

A. CNT DOS Simulation

The expression for the density of states shows van Hove singularities, which is characteristic of semiconductor material of CNT with (25, 0) is shown in Fig. 2. Fig. 2 represents the DOS graph for (25,0) where the band gap is 0.44eV. The presence of singularities in the density of states, the dependence of the bandgap on diameter, and the presence of semiconducting nanotubes become stable.

B. CNTFET I-V characteristics

Modeling of CNTFET with the I-V characteristics analysis is obtained for a channel length 14nm and width 2 times of length. For the 14nm gate length, we found a drive current I_D=720μA at V_{ds}=V_{gs}=0.4V and off-state current of 180 nA measured at V_g=0 and V_{ds}=0.4V, giving an I_{ON}/I_{OFF}= 4*103. The transconductance in the saturation region is gm=1.8 mS, which is found at Vds=0.4V for V_{gs}=V_{DD}=0.4V will minimize the ON/OFF current ratio. The resultant value is obtained of Sub-threshold swing is 36.0 mV/decade and DIBL is 54.73 mV/V.

C. Comparing Si MOSFETs and CNTFETs

The following parameters are necessary to compare CNTFET with Silicon MOSFET: (1) assess transistor performance at the transconductance (2) include both the on-state and off-state performance, and (3) fairly compare device metrics for different channel geometries/ channel length.

The analysis results in Fig. 3 and Fig. 4 show the drain current performance with the respect to the channel length of 14nm and width of 28nm the model is successfully analyzed. Comparison table1 also shows that higher frequency than existing CNTFET.

ISBN: 978-988-19252-0-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

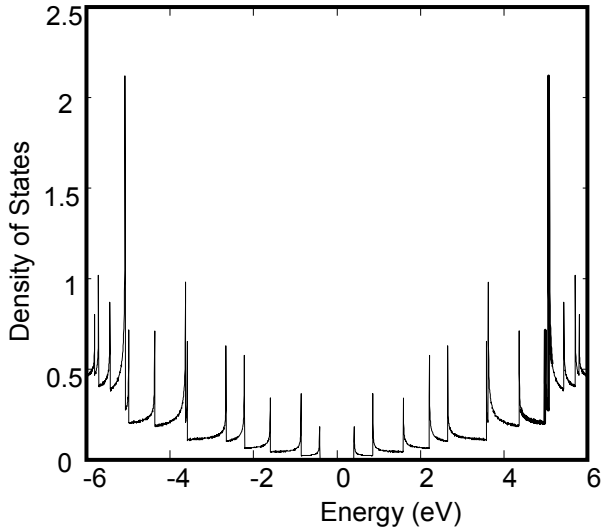

Fig. 2. DOS graph for (25,0) where the band gap is 0.44eV.

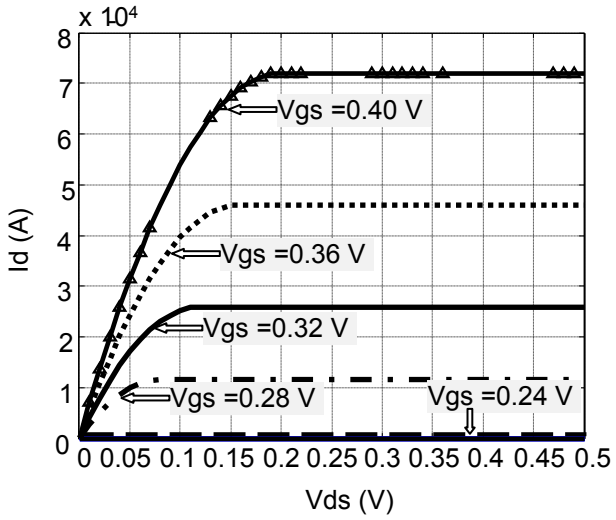

Fig. 3. CNTFET I-V Characteristics plot: drain current versus drain voltage.

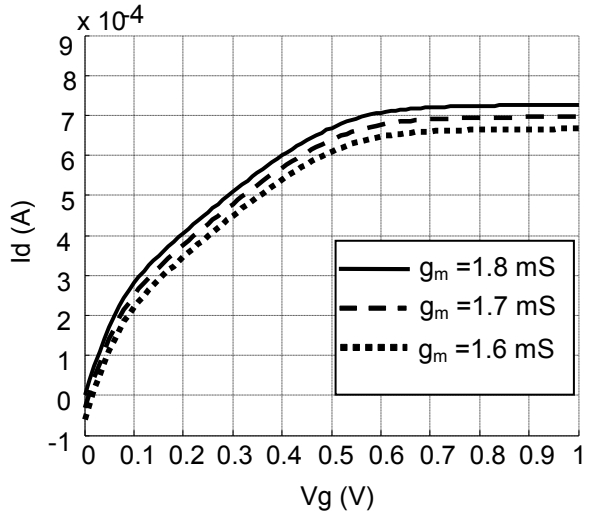

Fig. 4. CNTFET I-V Characteristics plot: drain current versus gate voltage.

TABLE I
COMPARISON BETWEEN PROPOSED AND EXISTING CNTFET

Parameter	CNTFET (this research)	CNTFET[20]
Channel length,L	14nm	45nm
Channel width,W	28nm	125nm
Channel area	$3.92*10^{-16}m^2$	$5.63*10^{-15}m^2$
Nanotube diameter	1.95nm	-
Chiral vector (n,m)	(25,0)	-
Current density,$I_d$max	720μA	50μA
Transconductance,gm	1.8 mS	148μS
Gate to source capacitance	14aF	65aF
Gate to drain capacitance	14aF	37aF
Cutoff frequency	10THz	27.72 Ghz
On-Off ratio	$4*10^3$	$9.54*10^5$
Subthreshold swing	36.0 mV/decade	113.67mV/decade
Drain-induced barrier lowering	54.73 mV/V	83.89mV/V
Power consumption	0.144mW	0.15mW

IV. CONCLUSIONS

This research reported a CNTFET model with the analysis of drain and gate voltage with respect to drain current. An experimental data was used to verify this analysis and shows that this new design reduces 4% of the power consumption from the existing model. Therefore, this proposed model can be used for semiconductor device production.

REFERENCES

[1] S. Borkar, "Design Challenges for 22nm CMOS and Beyond", IEDM09-446, 2009.
[2] D. L. John, L. C. Castro, and D. L. Pulfrey. "Quantum capacitance in nanoscale device modeling." Journal of Applied Physics 96.9 (2004): 5180-5184.
[3] J. Xiang, et al. "Ge/Si nanowire heterostructures as high-performance field-effect transistors." Nature 441.7092 (2006): 489-493.
[4] R. Baughman, A. Z. Anvar and W. A. de Heer. "Carbon nanotubes--the route toward applications." Science 297.5582 (2002): 787-792.
[5] C. D., Dimitrakopoulos, & P. R. Malenfant, Organic thin film transistors for large area electronics. Advanced Materials, 14(2), 99-117, 2002.
[6] S. J. Kang, C. Kocabas, T. Ozel, Shim, M., Pimparkar, N., Alam, M. A., J. A, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes", Nature Nanotechnology, 2(4), 230-236, 2007.
[7] S. Hasan, S. Salahuddin, M. Vaidyanathan, & M. A. Alam, "High-frequency performance projections for ballistic carbon-nanotube transistors", Nanotechnology, IEEE Transactions on, 5(1), 14-22, 2006.
[8] Q. Cao, H. Kim, N. Pimparkar, J.P. Kulkarni, C. Wang, M. Shim, & J.A. Rogers, "Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates", Nature, 454(7203), 495-500, 2008.
[9] X. Jiang, Shu-Shen Li, Jian-Bai Xia, and Lin-Wang Wang, "Quantum mechanical simulation of electronic transport in nanostructured devices by efficient self-consistent pseudopotential calculation", Journal of Applied Physics 109, 054503 (2011).
[10] G. Gelao, Roberto Marani, Roberto Diana, and Anna Gina Perri, "A Semiempirical SPICE Model for n-Type Conventional CNTFETs IEEE Transactions On Nanotechnology, Vol. 10, No. 3, May 2011.

ISBN: 978-988-19252-0-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

[11] S. Oh, Member, IEEE, and H.-S. Philip Wong, "Physics-Based Compact Model for III–V Digital Logic FETs Including Gate Tunneling Leakage and Parasitic Capacitance", IEEE Transactions On Electron Devices, Vol. 58, No. 4, April 2011.

[12] S. Farhana, A. Z. Alam, S. Motakabber and S. Khan, " Design and Analysis of CNT Electronics Structure to Design CNTFET," 5th IEEE International Nanoelectronics Conference, IEEE INEC 2013, 2013.

[13] S. Farhana, Z. Alam, S. Motakabber, and S. Khan. "Design and Development of a Simulator for Modelling Carbon Nanotube." In IOP Conference Series: Materials Science and Engineering, vol. 53, no. 1, p. 012049. IOP Publishing, 2013.

[14] S. Farhana, A. H. M. Alam, Sheroz Khan, and S. M. A. Motakabber. "Modeling of optimum chiral carbon nanotube using DFT", 13th IEEE Conference on Nanotechnology (IEEE-NANO), 2013 (2013): 853-857.

[15] S. Farhana, and A. H. M. Alam. "Environmental Friendly Device: Modeling of Carbon Nanotube with Optimum Chirality." Australian Journal of Basic & Applied Sciences 7, no. 8 (2013).

[16] S. Farhana, A. H. M. Zahirul Alam, Sheroz Khan, and S. M. A. Motakabber. "Modeling of small band-gap CNT for designing of faster switching CNTFET." In Business Engineering and Industrial Applications Colloquium (BEIAC), 2013 IEEE, pp. 589-592. IEEE, 2013.

[17] S. Farhana, A. H. M. Alam, and Sheroz Khan. "High frequency small signal modeling of CNTFET." IEEE Regional Symposium on Micro and Nanoelectronics (RSM), 2013 (2013): 364-367.

[18] S. Farhana, and AHM Zahirul Alam. "Modeling of a Carbon Nanotube Sensing Device." Middle-East Journal of Scientific Research 17, no. 10 (2013): 1475-1478.

[19] S. Farhana, A. H. M. Alam, Sheroz Khan, and S. M. A. Motakabber. "Investigation on carbon nanotube electronics structure." Pensee 75, no. 11 (2013): 123-129.

[20] A. Javey, R. Tu, Farmer DB, Guo J, Gordon RG, Dai H., "High performance n-type carbon nanotube field-effect transistors with chemically doped contacts", Nano Letters 2005, 5:345–348.

ISBN: 978-988-19252-0-6
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)